## REMARKS

Applicant has amended claims 8, 11, 48, 50, and 55 to correct typographical errors and antecedent basis. Note that the amendments to claims 8 and 11 are the same as previously submitted in the Amendment filed on February 23, 2005. They are re-submitted here because they were not acknowledged by the examiner in paragraph 1 of the Office Action mailed on August 9, 2005.

The Patent Office rejected claims 2-11 and 20-56 under 35 U.S.C. § 102(b) as being anticipated by Herold et al. (U.S. Patent No. 4,893,094), hereinafter referred to as Herold. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987).*

Regarding claim 2, Herold fails to expressly or inherently disclose configuring a main frequency divider of the synthesizer to operate as it had prior to deactivation of the synthesizer and activating the main frequency divider. Herold discloses a frequency synthesizer having sleep and awake cycles and including a phase locked loop. The voltage controlled oscillator (VCO) (36) is controlled by a control signal from storage unit (32). The storage unit (32) includes a capacitor (34) located between the charging circuit (28) and the VCO (36). During the sleep cycle, the VCO (36) and the reference oscillator (12) are deactivated to reduce the drain on the battery source. The capacitor (34) operates to store the control signal provided to the VCO (36) at the end of the previous awake cycle, and the control circuit (70) controls the charging circuit (28) such that the output line (30) of the charging circuit (28) is in a floating point state. As a result, the control signal remains stored on the capacitor (34) during the sleep cycle. Thereafter, when transitioning from the sleep cycle to the awake cycle, the VCO (36) is enabled, and the stored control signal is provided from the capacitor (34) to the VCO (36). The control circuit (70) controls the charging circuit (28) such that the output line (30) of the charging circuit (28) remains in the floating point state until both the VCO (36) and the reference oscillator (12) are initialized. Thereafter, the control circuit (70) activates the charging circuit (28), and the frequency synthesizer resumes normal operation.

However, Herold fails to disclose configuring the main frequency divider (44) to operate as it had prior to deactivation of the synthesizer or activating the main frequency divider (44) when activating the frequency synthesizer. In fact, Herold fails to disclose that the main

frequency divider (44) is ever deactivated. Herold only discloses that the VCO (36) and the reference oscillator (12) are deactivated during sleep mode. The main frequency divider (44) of Herold is always active. Since Herold fails to disclose deactivation of the main frequency divider (44), Herold also fails to disclose configuring the main frequency divider (44) to operate as it had prior to deactivation of the synthesizer and activating the main frequency divider (44). As such, claim 2 is allowable.

For at least the same reasons that claim 2 is allowable, claims 3-11 are also allowable. However, Applicant reserves the right to further address the rejections of claims 3-11 in the future if necessary.

Regarding claim 20, Herold fails to expressly or inherently disclose at least activating a main frequency divider such that it is initially out of phase with a reference frequency divider and activating a phase frequency detector after the main frequency divider is activated to receive input signals from the reference frequency divider and the main frequency divider. As discussed above, Herold does not disclose deactivating the main frequency divider (44) during sleep mode. As such, Herold fails to expressly or inherently disclose activating the main frequency divider (44). Still further, Herold fails to disclose activating the main frequency divider (44) such that it is initially out of phase with a reference frequency divider. As for activating the phase frequency detector, Herold discloses in the Abstract that the oscillators and the phase detector may be inhibited and enabled. However, Herold fails to disclose activating the phase frequency detector after the main frequency divider (44) is activated. As such, claim 20 is allowable.

For at least the same reasons that claim 20 is allowable, claims 21-24 are also allowable. However, Applicant reserves the right to further address the rejections of claims 21-24 in the future if necessary.

Regarding claim 25, Herold fails to expressly or inherently disclose at least control logic configured to inhibit the phase frequency detector, enable the first input signal to the phase frequency detector, enable the second input signal to the phase frequency detector, and activate the phase frequency detector. While the Abstract of Herold states that the phase detector may be inhibited and enabled, there is no other discussion of enabling or inhibiting the phase detector. Herold fails to disclose that the first and second input signals to the phase detector are enabled and then the phase detector is activated. In other words, Herold fails to disclose enabling the

first and second input signals to the phase detector before the phase detector is activated. As such, claim 25 is allowable.

For at least the same reasons that claim 25 is allowable, claims 26-37 are also allowable. However, Applicant reserves the right to further address the rejections of claims 26-37 in the future if necessary.

Regarding claim 38, Herold fails to expressly or inherently disclose at least a means for setting an operating frequency of the synthesizer device to a frequency the synthesizer device had operated at before being deactivated. Herold discloses activating the VCO (36) and reference oscillator (12) and controlling the charging circuit (28) such that the output of the charging circuit (28) is floating. As a result, the control signal stored by the capacitor (34) controls the VCO (36). Once the VCO (36) and reference oscillator (12) stabilize, the charging circuit (28) is activated and the synthesizer operates in a traditional fashion to set the operating frequency to a desired frequency. However, Herold fails to disclose that prior to setting the frequency to the desired frequency, the main frequency and reference dividers (44, 22) are configured such that the synthesizer operates at the operating frequency at which the synthesizer had operated prior to deactivation. As such, Herold fails to disclose a means for setting the operating frequency of the synthesizer device to a frequency the synthesizer device had operated at before being deactivated. Therefore, claim 38 is allowable.

For at least the same reasons that claim 38 is allowable, claims 39-43 are also allowable. However, Applicant reserves the right to further address the rejections of claims 39-43 in the future if necessary.

For reasons similar to those discussed above with respect to claim 25, claim 44 is allowable. For at least the same reasons that claim 44 is allowable, claims 45-47 are also allowable. However, Applicant reserves the right to further address the rejections of claims 45-47 in the future if necessary.

Regarding claim 48, Herold fails to expressly or inherently disclose at least activating the main frequency divider to provide an output signal to the phase frequency detector, wherein a phase of the output signal lags a phase of the reference signal. As such, claim 48 is allowable.

For at least the same reasons claim 48 is allowable, claims 49-56 are also allowable. However, Applicant reserves the right to further address the rejections of claims 49-56 in the future if necessary.

In view of the discussion above, claims 2-11 and 20-56 are allowable. Reconsideration is respectfully requested. If any issues remain, the examiner is encouraged to contact the undersigned attorney of record to expedite allowance and issue.

Respectfully submitted,

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